IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit 2616

In re application of	:	February 12, 2008
Patrick Lampin et al.	:	Examiner: Pawaris Sinkantarakorn
Serial No. : 10/605,049	:	
Filed: September 4, 2003	:	IBM Corporation Dept. 18G/Bldg, 300-482
Title: IMPROVED DYNAMIC TIME	:	2070 Route 52
DIVISION MULTIPLEXING	:	Hopewell Junction, NY
WITHOUT A SHADOW TABLE	:	12533-6531

APPEAL BRIEF

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the September 13, 2007 Final Rejection of claims 1 - 6. A correct copy of the claims is attached in the Claims Appendix.

Real Party in Interest

The real party in interest is International Business Machines Corporation per an assignment recorded in the US Patent and Trademark Office at Reel/Frame: 013935/0484 on September 4, 2003.

Related Appeals and Interferences

None.

Status of Claims

Claims 1 - 6 are pending. There are no other claims in the application.

Status of Amendments

No amendment after final rejection has been submitted.

Summary of the Claimed Subject Matter

The invention centers on the elimination of the need for a shadow table in a dynamic TDM system which uses a table of time slot assignment data (TSA) to determine which channels are allocated time slots in a bit-frame (transmitted or received). The invention eliminates the need for a shadow table by use of a Nx1 register indicating the status of the channel assignment data contained in the TSA table. The output of the register is provided to a set of p parallel AND gates (see reference numeral 41/ paragraph [0024]) which also receive a bit input of the p bits making up an entry in the TSA table where each table entry consists of p bits. See generally, paragraph [0010] of the specification

With respect to independent claim 1, the first data storage means comprising an n x p memory block is shown at reference numeral 31 in Figure 3 and discussed in the specification at paragraph [0022], line 2 where an example is indicated to be an SRAM; the second data storage means comprising a N x 1 register is shown at reference numeral 31 in Figure 3 and is discussed in the specification at paragraph [0022], line 3 and in other portions of paragraph [0022]; the input bus means for inputting the logical channel identifiers into said first data storage means is shown at reference numeral 34 in Figure 3 and discussed in the specification at paragraph [0022] 6th line from the end; logic circuit means connected to said first and second data storage means is shown at reference numeral 33 in Figure 3 and discussed in the specification at paragraph [0022] line

4 and in paragraph [0024] which shows a specific implementation of the logic circuit.

With respect to independent claim 6, the splitting time into time slots is described at paragraph [0003], [0004], and in Figure 3 in connection with memory block 31; storing in an N x p memory block time slot assignment (TSA) table is shown at reference numeral 31 and 34 in Figure 3 and discussed in paragraph [0022], storing status bits a register having N fields with a granularity of one bit is shown at reference numeral 32 and 34 in Figure 3 and discussed in paragraph [0022] , and transmitting said at least one identifier from said TSA table to a time slot assigner is shown at reference numeral 37 and 27 in Figure 3 and discussed in the specification at the end of paragraph [0025].

Grounds of Rejection to be Reviewed on Appeal

1. Claims 1 - 6 are rejected under 35 USC 103(a) as being unpatentable over the admitted prior art in view of US Pat. 7,042,895 (Nguyen et al.).

Argument

1. Claims 1 - 6 are rejected under 35 USC 103(a) as being unpatentable over the admitted prior art in view of US Pat. 7,042,895 (Nguyen et al.).

The admitted prior art discloses a dynamic TDM system where a TSA table and a shadow TSA table are used to provide flexibility to the dynamic TDM system. The admitted prior art does not disclose or suggest how to obtain the flexibility of dynamic TDM without use of a shadow TSA table. The admitted prior art does not disclose or suggest the use of an N x 1 bit register in combination with a TSA table. The admitted prior art does not disclose or suggest inputting bits from p bit channel

identifiers into p parallel AND gates. The admitted prior art does not disclose or suggest the inputting of a register bit value into p parallel AND gates.

Nguyen et al. disclose a method of controlling the transmission of data from a set of modems (handling n-bit words) using a tri-state buffer in combination with a shift register whose output is controlled by channel clock signal operating at 1/n speed of the data clock wherein the shift register output is fed with the modem data to an XOR gate. Nguyen et al. does not disclose or suggest use of resister in combination with a table of time slot assignment data. Nguyen et al. does not disclose or suggest the use of a parallel group of AND gates, nor the feeding of bits of p bit TSA time slot data to p parallel AND gates, nor the feeding of bits from an N x 1 register to the same AND gates.

Appellants submit that the combination of the teachings of Nguyen et al. with the admitted prior art would have either resulted modification of the admitted prior art to convert it to a static TDM system (i.e., the Nguyen-type system) or the modification of the interaction of the time slot assigner with the FIFOs containing or receiving data from the respective channels of the system. In either event, appellants submit that that combination would not result in the claimed invention.

The office action postulates that there would be motivation to incorporate the register of Nguyen et al. into the admitted prior art shadow table TDM, but the referenced motivation of col. 5, line 21-23 of Nguyen et al. is referring to the systems of Nguyen et al., not to the systems of the admitted prior art. It is not apparent how one of ordinary skill in the art would integrate the teaching of Nguyen et al. with the admitted prior art to achieve elimination of the shadow table as provided by the present invention.

Conclusion

Based on the above arguments, appellant submits that the present claims are patentable over the prior art of record and that the rejection under 35 USC 35 USC 103(a) should be reversed.

Respectfully submitted,
Patrick Lampin et al.

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Claims Appendix

Claims on Appeal

1. In a telecommunication system split into a plurality of subsystems to exchange serial data bits arranged in frames n bits long (n-bit frames) according to a dynamic time division multiplexing (TDM) access method wherein the time is split in time slots, so that to each bit position (Bit1 to Bitn) of said frame is associated either one among N logical channels or a null value, N being the maximum number of logical channels that can be simultaneously opened and wherein to each logical channel (X) is associated an identifier (LC X) coded on p bits where N, n and p are integers, wherein the improvement comprises:

first data storage means comprising an n x p memory block to store a time slot assignment (TSA) table which specifies for each bit position of the n-bit frame, the logical channel it belongs to at a given time, describing thereby the different time slots;

second data storage means comprising a N x 1 register to store status bits that indicates for each logical channel its status, “assigned” when it has a first value or “unassigned” when it has another value;

input bus means for inputting the logical channel identifiers into said first data storage means and the value of the status bits in said second data storage means from a computer or an application software; and,

logic circuit means connected to said first and second data storage means that enables or disables the transmission of the logical channel identifiers

depending upon they are “assigned” or “unassigned” to an output bus means for subsequent processing by a time slot assignor.

2. The telecommunication system according to claim 1 wherein the null value corresponds to a bit position to which no logical channel is assigned.

3. The system of claim 1 wherein said logic circuit means comprises p parallel two-way AND gates.

4. The system of claim 3 wherein said AND gates receive inputs from said memory block and from said register.

5. The system of claim 4 wherein each AND gate receives one of p bits from a channel identifier data entry in said TSA table.

6. A method for providing logical channel identifier information to a time slot assignor in a dynamic time division multiplexing process, said method comprising:

splitting time into time slots, each slot corresponding to one among N logical channels, wherein N is a maximum number of logical channels that can be simultaneously opened in said process,

storing in an N x p memory block time slot assignment (TSA) table at least one identifier (LC X) associated with logical channel (X), each said identifier being coded on p bits, specifying each bit position of an n-bit TDM frame that is assigned to said logical channel,

storing status bits a register having N fields with a granularity of one bit, each bit indicating the status of a corresponding identifier in said TSA table, and

transmitting said at least one identifier from said TSA table to a time slot assigner, wherein said transmission is controlled by a logic circuit receiving data from said resister as an input thereto.

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Evidence Appendix

None.

[End of Evidence Appendix]

Related Proceedings Appendix

None.

[End of Related Proceedings Appendix]